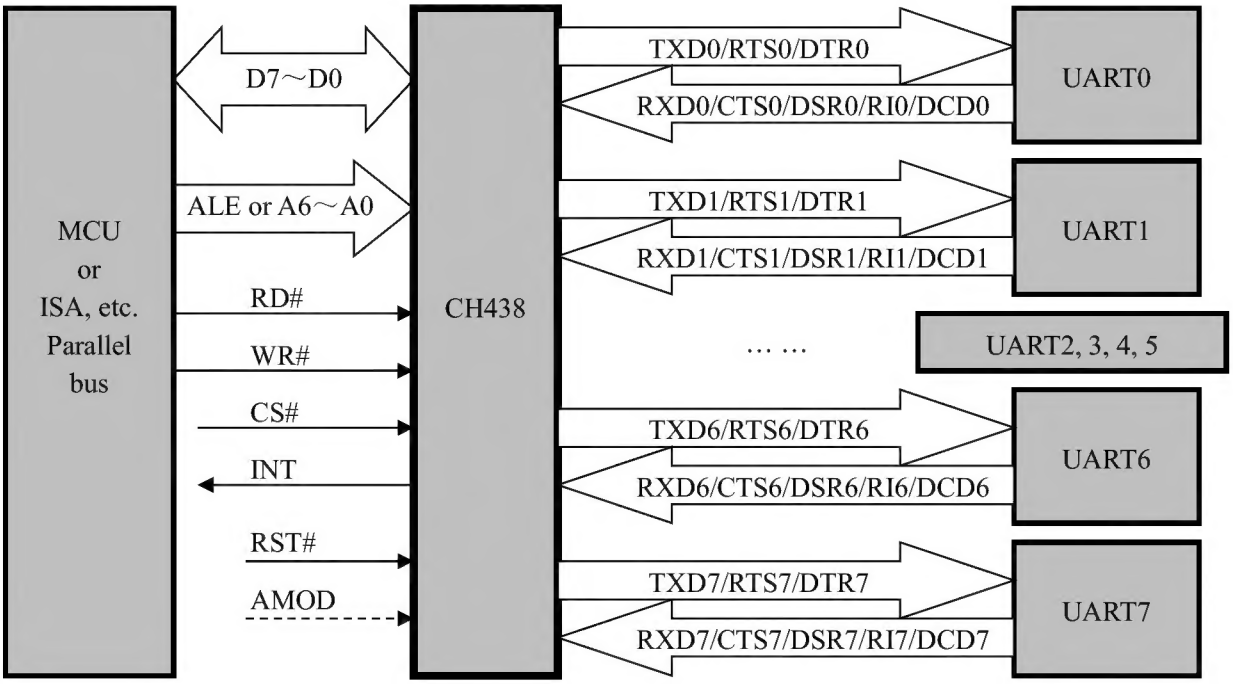
8-UART Chip CH438

Datasheet
Version: 1B
http://wch.cn

1. Overview

CH438 is an eight-UART chip, which contains eight UARTs compatible with 16C550 or 16C750 and supports the communication baud rate up to 4Mbps. It can be used for RS232 extension of MCU/embedded system, high-speed UART with automatic hardware rate control, RS485 communication, etc. The figure below shows its general application block diagram.



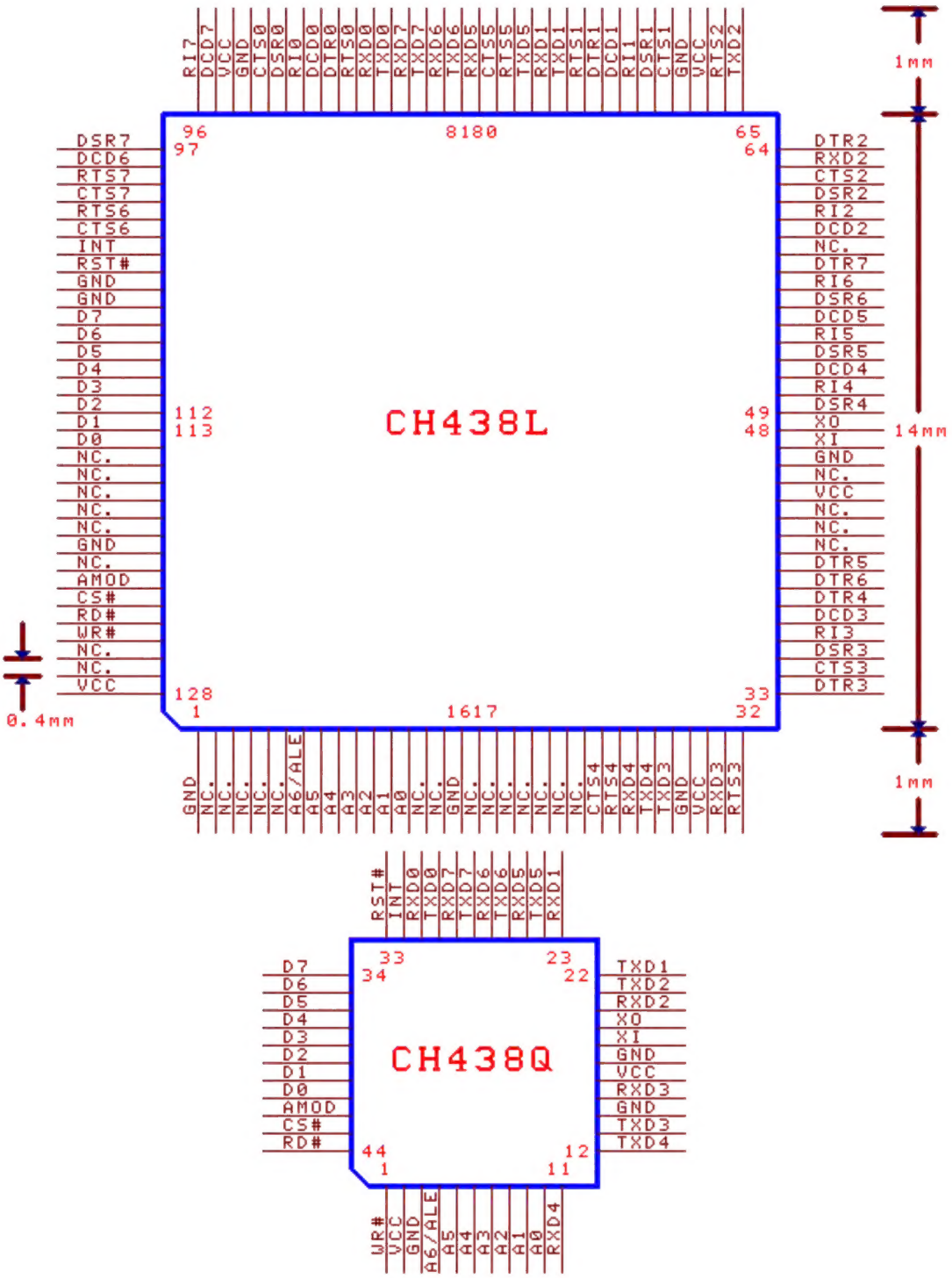
2. Features

- Eight fully independent UARTs, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Support 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Support the verification modes of odd, even, null verification, blank 0 and flag 1.
- Programmable communication baud rate, support communication baud rate of 115200bps and up to 4Mbps.
- Built-in 128-byte FIFO buffer, support four FIFO trigger levels.
- Support MODEM signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 level by 75232 chip.
- Support automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Support serial port frame error detection and Break line interval detection.
- Built-in clock oscillator, supporting the crystal with frequency range of 0.9216MHz-32MHz, using 22.1184MHz crystal by default.
- Provide 10MB 8-bit passive parallel interface to connect MCU.
- The parallel interface contains an 8-bit data bus, a 7-bit address, and a 3-wire control: chip selection input, write strobe and optional read strobe.
- Support direct and multiplexed addresses: input the 7-bit address directly or latch the address by

ALE signal control from the data bus.

- The interrupt output pin is an optional connection and is active at low level. It can be replaced by querying the interrupt flag bit in the register.
- Support 5V or 3.3V supply voltage and support serial port low-power sleep mode.
- Provide LQFP-44 and LQFP-128 lead-free package, and be compatible with RoHS.

3. Package



Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
LQFP-128	14mm x 14mm	0.4mm	15.7mil	Standard LQFP128-pin patch	CH438L
LQFP-44	10mm x 10mm	0.8mm	31.5mil	Standard LQFP 44-pin patch	CH438Q

4. Pins

CH438Q chip is a compact version when MODEM signal pins are removed from CH438L chip. Except for MODEM signal pins, other functions are exactly the same. The homonymous pins of CH438Q has the same functions, and only CH438L is taken as an example in the following pin description.

4.1. Power Supply and System Signal Line

Pin No.	Pin name	Type	Pin description
30, 44, 67, 94, 128	VCC	Power	Positive power terminal
1, 16, 29, 46, 68, 93, 105, 106, 120	GND	Power	Common grounding end
2-6, 14, 15, 17-23, 41-43, 45, 58, 115-119, 121, 126, 127	NC.	Idle pin	Connection disabled
47	XI	Input	Input terminal of the crystal oscillator, required to be connected to an external crystal and oscillation capacitor
48	XO	Output	Reverse-phase output terminal of the crystal oscillator, required to be connected to an external crystal and oscillation capacitor

4.2. MCU Interface Signal Wire

Pin No.	Pin name	Type	Pin description
104	RST#	Input	External manual reset input, active at low level, built-in weak pull-down resistor
122	AMOD	Input	Address input mode selection: Low level is the direct address mode, and high level is the multiplexed address mode
107-114	D7～D0	Three-status output and input	8-bit parallel bidirectional data signal line Address and data multiplexing signal line in multiplexed address mode
7-13	A6～A0	Input	Address line input in direct address mode
7	ALE	Input	Address latch enabling input in multiplexed address mode, active at high level
124	RD#	Input	Read strobe input in parallel port mode, active at low level
125	WR#	Input	Write strobe input in parallel port mode, active at low level
123	CS#	Input	Chip selection control input in parallel port mode, active at low level
103	INT	Open-drain output	Interrupt request output, active at low level, pull-up resistor may be required to be externally connected

4.3. UART Signal Line

Pin No.	Pin name	Type	Pin description
92/69 62/34 24/79 102/100	CTS0/CTS1 CTS2/CTS3 CTS4/CTS5 CTS6/CTS7	Input	MODEM signal, clear sending, active at low level, built-in weak pull-up resistor CH438Q does not have this pin
91/70 61/35 49/52 55/97	DSR0/DSR1 DSR2/DSR3 DSR4/DSR5 DSR6/DSR7	Input	MODEM signal, data device ready, active at low level, built-in weak pull-up resistor CH438Q does not have this pin
90/71 60/36 50/53 56/96	RI0/RI1 RI2/RI3 RI4/RI5 RI6/RI7	Input	MODEM signal, ringing indication, active at low level, built-in weak pull-up resistor CH438Q does not have this pin
89/72 59/37 51/54 98/95	DCD0/DCD1 DCD2/DCD3 DCD4/DCD5 DCD6/DCD7	Input	MODEM signal, carrier detection, active at low level, built-in weak pull-up resistor CH438Q does not have this pin
86/76 63/31 26/80 82/84	RXD0/RXD1 RXD2/RXD3 RXD4/RXD5 RXD6/RXD7	Input	Asynchronous serial data input, built-in weak pull-up resistor
88/73 64/33 38/40 39/57	DTR0/DTR1 DTR2/DTR3 DTR4/DTR5 DTR6/DTR7	Output	MODEM signal, data terminal ready, active at low level CH438Q does not have this pin
87/74 66/32 25/78 101/99	RTS0/RTS1 RTS2/RTS3 RTS4/RTS5 RTS6/RTS7	Output	MODEM signal, request sending, active at low level CH438Q does not have this pin
85/75 65/28 27/77 81/83	TXD0/TXD1 TXD2/TXD3 TXD4/TXD5 TXD6/TXD7	Output	Asynchronous serial data output

5. Internal Clock Configuration

CH438 has a clock oscillator inside. The external clock signal required by the serial port can be generated only by connecting a crystal between XI and XO pins and connecting the oscillating capacitor for XO pins to the ground. If the crystal and the capacitor are not connected, CH438 can also directly input the clock from the external clock source through XI pin.

CK2X is the bit 5 of IER register for the UART1 - UART7. The internal CK2X of CH438 selects the external clock signal of XI pin to perform 1/12 frequency division or frequency doubling, and the generated internal reference clock is provided to the UART0 - UART7. CK2X is 0 by default. If CK2X is 0, 1/12 frequency division will be selected; if CK2X is 1, frequency doubling will be selected. If it is necessary to be compatible with the existing 16C550 serial port chip, the internal clock frequency shall be 1.8432MHz and the corresponding maximum serial port baud rate shall be 115200bps, so the default external clock frequency is 22.1184MHz. If a high serial port baud rate is required, set CK2X to 1 and select a high external clock frequency. If a serial port baud rate with a special value is required, an external clock or crystal with a

specific frequency shall be selected.

UART0 of CH438 only supports 1/12 frequency division of an internal clock frequency, and does not support frequency doubling, and UART1 - UART7 support CK2X to select frequency division or frequency doubling. The following table shows the internal clock frequency and maximum serial port Baud rate of the serial port generated from UART1 - UART7 according to CK2X value and external crystal frequency.

External input clock frequency or external crystal frequency	CK2X=0, internal 1/12 frequency division		CK2X=1, internal frequency doubling	
	Internal clock frequency	Maximum baud rate	Internal clock frequency	Maximum baud rate
32MHz			64MHz	4Mbps
22.1184MHz	1.8432MHz	115.2Kbps	44.2368MHz	2.7648Mbps
18.432MHz			36.864MHz	2.304Mbps
14.7456MHz			29.4912MHz	1.8432Mbps
11.0592MHz	0.9216MHz	57.6Kbps	22.1184MHz	1.3824Mbps
7.3728MHz	0.6144MHz	38.4Kbps	14.7456MHz	921.6Kbps
3.6864MHz	0.3072MHz	19.2Kbps	7.3728MHz	460.8Kbps
0.9216MHz			1.8432MHz	115.2Kbps

6. Registers

CH438 has 8 independent UART modules. In the register address space distribution, each UART occupies 8 bytes of address space. Address 00H-07H is the register of UART0, address 08H-0FH is the register of UART4, address 10H-17H is the register of UART1, address 18H-1FH is the register of UART5, address 20H-27H is the register of UART2, address 28H-2FH is the register of UART6, address 30H-37H is the register of UART3, and address 38H-3FH is the register of UART7. In addition, the register of address 4FH is a special state register (SSR), which is a read-only register and used to query the interrupt status of UART0 - UART7 inside the chip.

6.1. Special State Registers

The special state register for CH438 is a read-only register with an address of 4FH.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	S7INT	S6INT	S5INT	S4INT	S3INT	S2INT	S1INT	S0INT

SSR: special state register, used to query each interrupt state inside the chip, etc. 1 indicates that interrupt is being requested.

S7INT: The bit is the interrupt request state of UART7.
S6INT: The bit is the interrupt request state of UART6.
S5INT: The bit is the interrupt request state of UART5.
S4INT: The bit is the interrupt request state of UART4.
S3INT: The bit is the interrupt request state of UART3.
S2INT: The bit is the interrupt request state of UART2.
S1INT: The bit is the interrupt request status of UART1.
S0INT: The bit is the interrupt request status of UART0.

6.2. Serial Port Registers

The serial port of CH438 is compatible with the industry standard 16C550 or 16C750 and has been enhanced. The register bit marked in gray in the table is the enhanced function, and the length of FIFO buffer is extended to 128 bytes. Refer to the description of the single serial port chip16C550 for other registers.

Except for start addresses, the registers of UART1 and UART2, UART3, UART4, UART5, UART6 and UART7 are all the same. Except for SLP/CK2X register bit, the registers of UART0 and UART1 are the

same. In the table, DLAB is bit 7 of the register LCR, X means that the value of DLAB is not concerned, RO means the register is read-only, WO means the register is write-only, and R/W means the register is readable and writable.

Address	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RO	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WO	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	SLP/CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	0	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	0	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	0	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	△DCD	△RI	△DSR	△CTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table shows the default of the serial port register after external manual reset or serial port soft reset.

Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Keep	Keep	Keep	Keep	Keep	Keep	Keep	Keep
FIFO	Reset, including FIFO transmitting and FIFO receiving							
TSR	Reset; TSR is the UART transmitter shift register							
RSR	Reset; RSR is the UART receiving shift register							
Other	is not defined							

RBR: Receiving buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this register. If FIFOEN is 1, the data received from the UART shift register RSR will be firstly stored in the receive FIFO, and then read out through the register.

THR: Transmitter hold register, including transmit FIFO, for writing the data to be transmitted. If FIFOEN is 1, the written data will be firstly stored in the transmit FIFO, and then output one by one through the transmitter shift register TSR.

IER: Interrupt enabling register, including enhanced function control bit and serial port interrupt enabling.

RESET: When this bit is set to 1, soft reset the serial port, and this bit can be cleared automatically without software clearing.

LOWPOWER: When this bit is 1, the internal reference clock of the serial port will be turned off, so that the serial port will enter a low power consumption status.

SLP/CK2X: the purpose of UART0 at the bit is different from UART1- UART7, and UART0 is SLP. When the bit is 1 and LOWPOWER is 1, turn off the clock oscillator, so that all UARTs sleep. UART1- UART7 are CK2X. When the bit is 1, force the external clock signal for frequency doubling and then use it as the internal reference clock of UART1- UART7.

IEMODEM: When this bit is 1, it will allow modem input status change interrupt.

IELINES: When this bit is 1, it will allow receiver line status interrupt.

IETHRE: When this bit is 1, it will allow transmitter hold register null interrupt.

IERECV: When this bit is 1, it will allow received data interrupt.

IIR: Interrupt recognition register, for analyzing the interrupt source and processing.

FIFOENS: This bit is the FIFO enabled status, and 1 means that the FIFO has been enabled.

IIR register bit				Priority	Interrupt type	Interrupt sources	Clearing interrupt method
IID3	IID2	IID1	NOINT				
0	0	0	1	None	No interrupt generated	No interrupt	
0	1	1	0	1	Receiving line status	OVERR、PARERR、FRAMEERR、BREAKINT	Reading LSR
0	1	0	0	2	Receiving data available	The number of bytes received reaches the trigger point of FIFO	Reading RBR
1	1	0	0	2	Data receiving timeout	No next data is received when the time of four data is exceeded	Reading RBR
0	0	1	0	3	THR register null	Transmitter hold register null, IETHRE changes from 0 to 1 to re-enable the interrupt	Reading IIR Or writing THR
0	0	0	0	4	MODEM input change	△CTS、△DSR、△RI、△DCD	Reading MSR

FCR: First-in-first-out buffer area FIFO control register, used to enable and reset FIFO.

RECVTG1 and RECVTG0: Set the trigger point for receive FIFO interrupt and hardware flow control. 00 corresponds to 1 byte, that is, interrupt available for receiving data is generated when a byte is received, and RTS pin is automatically invalid when hardware flow control is enabled. 01 corresponds to 16 bytes, 10 corresponds to 64 bytes, and 11 corresponds to 112 bytes.

TFIFORST: When this bit is set to 1, the data in the FIFO transmitting (not including TSR) will be cleared. This bit can be cleared automatically without software clearing.

RFIFORST: When this bit is set to 1, the data in the FIFO transmitting (not including RSR) will be cleared. This bit can be cleared automatically without software clearing.

FIFOEN: When this bit is 1, FIFO will be enabled. When this bit is cleared, FIFO will be disabled. After FIFO is disabled, it will be 16C450 compatible mode, which is equivalent to only one byte in FIFO (RECVTG1=0, RECVTG0=0, FIFOEN=1). It is suggested that FIFO shall be enabled.

LCR: Line control register, used to control the format of serial communication.

DLAB: This bit is the access enabling of the divisor latch. When it is 1, DLL and DLM can be accessed; when it is 0, RBR/THR/IER can be accessed.

BREAKEN: When this bit is 1, it is mandatory to generate a BREAK line interval.

PARMODE1 and PARMODE0: When PAREN is 1, set the format of the parity bit: 00 means odd parity, 01 means even parity, 10 means mark bit (MARK, set to 1), 11 means blank bit (SPACE, cleared).

PAREN: When this bit is 1, it is allowed to generate parity bit during transmission and check parity bit when receiving. If it is 0, there is no parity bit.

STOPBIT: When this bit is 1, there will be two stop bits. When it is 0, there will be one stop bit.

WORDSZ1 and WORDSZ0: Set the word length; 00 means 5 data bits, 01 means 6 data bits, 10 means 7 data bits, and 11 means 8 data bits.

MCR: Modem control register, used to control MODEM output.

AFE: When this bit is 1, the hardware automatic flow control of CTS and RTS is allowed. If AFE is 1, then the serial port will continuously send the next data only when it detects that the CTS pin input is valid (active at low level). Otherwise, the serial port transmission will be suspended, and the CTS

input status change will not generate the MODEM status interrupt when AFE is 1. If AFE is 1 and RTS is 1, the serial port will automatically validate the RTS pin (active at low level) when receive FIFO is null. The serial port will automatically invalidate the RTS pin when the number of received bytes reaches the trigger point of FIFO and will re-validate the RTS pin when the receive FIFO is null. You can connect your own CTS pin to the other party's RTS pin through the hardware automatic band rate control, and can connect your own RTS pin to the other party's CTS pin.

LOOP: When this bit is 1, the test mode of the internal loop will be enabled. In the test mode of the internal loop, all external output pins of the serial port are at the invalid status, TXD internally returns to RXD (i.e., the output of TSR internally returns to the input of RSR), RTS internally returns to CTS, DTR internally returns to DSR, OUT1 internal returns to RI and OUT2 internally returns to DCD.

OUT2: If this bit is 1, the interrupt request output of the serial port is allowed. Otherwise, the serial port will not generate the actual interrupt request.

OUT1: This bit is a user-definable MODEM control bit, and no actual output pin is connected.

RTS: If this bit is 1, the RTS pin output will be valid (active at low level). Otherwise, the RTS pin output will be invalid.

DTR: If this bit is 1, the DTR pin output will be valid (active at low level). Otherwise, the DTR pin output will be invalid.

LSR: Line status register, used for querying and analyzing the status of the serial port.

RFIFOERR: When this bit is 1, it means that there is at least one PARERR, FRAMEERR or BREAKINT error in the receive FIFO.

TEMT: When this bit is 1, it means that the transmitter hold register (THR) and the transmitter shift register (TSR) are both null.

THRE: When this bit is 1, it means that the transmitter hold register (THR) is null.

BREAKINT: When this bit is 1, it means that the BREAK line interval is detected.

FRAMEERR: When this bit is 1, it means the frame error of the data being read from the receive FIFO due to lack of a valid stop bit.

PARERR: When this bit is 1, it means the parity error of the data being read from the receive FIFO.

OVERR: When this bit is 1, it means that the receive FIFO buffer area has overflowed.

DATARDY: When this bit is 1, it means that there is received data in the receive FIFO. After reading all the data in the FIFO, this bit will be automatically cleared.

MSR: Modem status register, used to query the Modem status.

DCD: This bit is the reverse bit of the DCD pin. When it is1, it means that the DCD pin is valid (active at low level).

RI: This bit is the reverse bit of RI pin. When it is 1, it means that RI pin is valid (active at low level).

DSR: This bit is the reverse bit of DSR pin. When it is 1, it means that DSR pin is valid (active at low level).

CTS: This bit is the reverse bit of CTS pin. When it is 1, it means that CTS pin is valid (active at low level).

△DCD: When this bit is 1, it means that the DCD pin input status has changed.

△RI: When this bit is 1, it means that the input status of the RI pin has changed.

△DSR: When this bit is 1, it means that the input status of the DSR pin has changed.

△CTS: When this bit is 1, it means that the input status of the CTS pin has changed.

SCR: The user can define the register.

DLL and DLM: Baud rate divisor latch. DLL is the low byte and DLM is the high byte. The 16-bit divisor formed by the two is used for the serial port baud rate generator composed of a 16-bit counter. The divisor = the internal reference clock of UART / 16 / the required communication baud rate. If the internal reference clock of UART is 1.8432MHz and the required baud rate is 9600bps, then the divisor =1843200/16/9600=12.

7. Function Description

7.1. Query and Interrupt

The 8 UARTs of CH438 use one interrupt request pin INT, so MCU shall first analyze which UART has the interrupt request after inputting the interrupt service program. After inputting the interrupt service program, there are two methods: dedicated status analysis and sequential query:

Special state analysis means the first reading of special state register SSR first. S0INT valid indicates that UART0 is interrupted, S1INT valid indicates that UART1 is interrupted, S2INT valid indicates that UART2 is interrupted, S3INT valid indicates that UART3 is interrupted, S4INT valid indicates that UART4 is interrupted, S5INT valid indicates that UART5 is interrupted, S6INT valid indicates that UART6 is interrupted, and S7INT valid indicates that UART7 is interrupted. Directly process according to the analysis result. Directly exit in case of no interrupt.

Sequential query means the first reading of UART0 IIR register. Process and exit in case of interrupt. Read the IIR register of UART1 in case of no interruption. Process and exit it in case of interrupt. Read the IIR register of UART2 in case of no interrupt. Process and exit in case of interrupt. Read the IIR register of UART3 in case of no interrupt. In the same way, process and exit in case of interrupt. Read the IIR register of UART7 in case of no interrupt. Process and exit in case of interrupt. Directly exit in case of no interrupt.

After ensuring that it is an interrupt of a certain UART, you can further analyze the LSR register, analyze the cause of the interrupt and process it if necessary.

If UART works in the interrupt mode, you need to set the IER register to allow the corresponding interrupt request, and set OUT2 in the MCR register to allow interrupt output. Interrupt request pin INT is an active low open-drain output pin, which may be required to be attached with a pull-up resistor when being connected to MCU. In function, INT is "or not" of each UART interrupt.

If UART works in query mode, then no OUT2 of IER and MCR are required to be set. You only need to query the LSR register and analyze and process it.

7.2. Serial Port Operation

Transmitter hold register (THR) empty interrupt sent by the UART (the low 4 bits of IIR are 02H) refers to transmitter FIFO empty. The interrupt is cleared when the IIR is read, or the interrupt may be cleared when the next data is written to THR. If only one byte is written to THR, CH438 will soon generate a request of "transmitter hold register (THR) empty interrupt" as the byte is quickly transferred to the transmitter shift register (TSR) to start transmitting. At this point, the next data ready to be transmitted can be written. After all the data in TSR is removed, UART sending is completed and valid when TEMT bit of LSR is 1.

When MCU receives the THR empty interrupt from UART, if FIFO is enabled, up to 128 bytes can be written to THR and FIFO at a time and will be transmitted automatically by CH438 in sequence. If FIFO is disabled, only one byte can be written at a time. If no data needs to be transmitted, simply exit (the interrupts have been automatically cleared when IIR is read earlier).

In the query mode, MCU can judge whether the transmitter FIFO is null according to THRE bit of LSR. If THRE is 1, it can write data to THR and FIFO. If FIFO is enabled, it can write up to 128 bytes at a time.

Data availability interrupt received by UART (the low 4 bits of IIR are 04H) means that the number of existing data bytes in the receiver FIFO has reached or exceeded the FIFO trigger points selected by RECVTG1 and RECVTG0 of FCR. The interrupt is cleared when the data is read from RBR to cause the number of bytes in the FIFO below the FIFO trigger points. Data timeout interrupt received by UART (the low 4 bits of IIR are 0CH) means that there is at least one byte of data in the receiver FIFO, and the user has waited for the time equivalent to the time for receiving 4 data when UART receives data last time and MCU takes the data last time. The interrupt is cleared when a new data is received again, or the interrupt can also be cleared when MCU reads RBR once. When receiver FIFO is empty, DATARDY bit of LSR is 0; when there are data in the receiver FIFO, DATARDY bit is 1.

When MCU receives the serial data receiving timeout interrupt, it can first read a byte from RBR, and then query DATARDY bit of LSR. If DATARDY bit is valid, it will read another byte until DATARDY bit is

invalid.

When MCU receives the serial data availability interrupt, first read the number of bytes set by RECVTG1 and RECVTG0 of RBR, and then query DATARDY of LSR. If DATARDY bit is valid, read a byte again until DATARDY bit is invalid, or read after querying that LSR DATARDY bit is valid.

In the query mode, MCU can judge whether the receiver FIFO is empty according to DATARDY bit of LSR. If DATARDY bit is 1, read a byte of data from RBR and then query the status of DATARDY bit. If it is valid, read RBR again until DATARDY bit is 0.

Receiver line status interrupt (IIR low 4 bits are 06H) means that CH438 detects errors or exceptions in the serial receiving process after MCU reads LSR last time. When the line status is read from LSR, the interrupt and the status bit in LSR are cleared. The interrupt is logic "or" for the bit data BREAKINT, FRAMEERR, PARERR and OVERR of LSR.

MODEM input change interrupt (the low 4 bits of IIR are 00H) means that CH438 detects the change of MODEM input signal after MCU reads MSR last time. When MODEM status is read from MSR, the interrupt and the status bit in MSR are cleared. The interrupt is logic "or" for the bit data △DCD, △RI, △DSR and △CTS of MSR.

7.3. Hardware Flow Control

Hardware flow control includes automatic CTS (AFE of MCR is 1) and automatic RTS (AFE and RTS of MCR are 1).

If automatic CTS is enabled, CTS pin must be valid before UART sends data. UART transmitter detects CTS pin before sending the next data. When CTS pin state is valid, the transmitter sends the next data. In order to ensure that the transmitter stops sending the later data, CTS pin must be disabled before the middle of the last stop bit currently sent. The automatic CTS function reduces the interrupt applied to MCU system. When hardware flow control is enabled, a change in CTS pin level does not trigger a MODEM interrupt as CH438 automatically controls the transmitter based on CTS pin status.

If automatic RTS is enabled, RTS pin output will be valid only when there is enough space in FIFO to receive data, and RTS pin output is disabled when the receiver FIFO is full. RTS pin output will be valid if all the data in the receiver FIFO is taken or cleared. When the trigger points for the receiver FIFO are reached (the number of existing bytes in the receiver FIFO is not less than the number of bytes set by RECVTG1 and RECVTG0 of FCR), RTS pin output is invalid, and the transmitter of the other side is allowed to send another data after RTS pin is invalid. Once the data in the receiver FIFO is emptied, RTS pin will be automatically re-enabled, so that the transmitter of the other side restores sending.

If both automatic CTS and automatic RTS are enabled (both AFE and RTS of MCR are 1), one side will not send data unless there is sufficient space in the receiver FIFO of the other side when RTS pin of one side is connected to CTS pin of the other side. Therefore, the hardware flow control of CH438 can avoid FIFO overflow and timeout errors during serial receving.

7.4. MCU Interfaces

CH438 provides a universal 8-bit passive parallel interface at the local terminal, which supports two address input modes: direct address and multiplexed address. When AMOD pin is at low level, select the direct address mode; when AMOD pin is at high level, select multiplexed address mode.

The parallel port signal line includes: 8-bit bidirectional data buses D7-D0, read strobe input pin RD#, write strobe input pin WR#, chip selection input pin CS# and address input pin A6-A0 or address latch enable pin ALE. CH438 can be easily hooked to the system buses of various 8-bit MCUs, DSP and MCU through a passive parallel interface, and can coexist with multiple peripheral devices.

CS# pin of CH438 is driven by the address decoding circuit, and can be used for device selection when MCU has multiple peripheral devices. When there is only one peripheral device, CS# pin can be connected to the low level or GND to remain selected.

For MCU similar to the Intel parallel port timing sequence, RD# and WR# pins of CH438 can be connected to the read strobe output pin and write strobe output pin of MCU respectively. For MCU similar to

Motorola parallel port timing sequence, RD# pin of CH370 chip shall be connected to the low level, and WR# pin shall be connected to the read and write direction output pin R/-W of MCU.

In the direct address mode, the current operation address is input directly by the pins A6-A0 during the access operation.

In the multiplexed address mode, the current operation address is input and latched from the pins D6-D0 during ALE pin high level before the access operation. ALE pin is an alias for the pin A6. When ALE pin is at high level, data appearing on the pins D6-D0 is used as address latch. ALE pin shall be at low level during access operation, so previously latched addresses are not affected.

The following table is the truth table of the parallel port I/O operation (X in the table means that this bit is not concerned, and Z means that three states of CH438 are disabled).

CS#	WR#	RD#	D7-D0	Actual operation on CH438
1	X	X	X/Z	CH438 is not selected, and no any operation is made
0	1	1	X/Z	Although selected, no any operation is made
0	0	X	Input	Write data to the specified address of CH438
0	1	0	Output	Read data from the specified address of CH438

7.5. Application Specifications

The output pins of CH438 are at CMOS level, compatible with TTL levels, and the input pins are compatible with CMOS and TTL levels, and can be further converted to RS232 by adding an RS232 level converter externally. Any pins of CH438 not used in the actual circuit can be suspended.

When UART of CH438 works normally, the clock signal shall be externally provided for XI pin. Generally, the clock signal is generated by the built-in inverter of CH438 through the crystal stable frequency oscillator. To reduce power consumption, if only one UART is used, LOWPOWER bit of IER for other UARTs can be set to 1 and the unused UARTs can be turned off; if all UARTs are temporarily out of use, SLP bit and LOWPOWER bit of IER for the UART0 can be set to 1, and the clock oscillator can be turned off. However, when the clock oscillator is turned on again, it is necessary to wait for the start and stabilization time of at least 3 milliseconds before the serial port operation.

The UART pins of CH438 include: data transmission pin and MODEM contact signal pin. Data transmission pins include: TXD pin and RXD pin. When UART is idle, TXD and RXD are at high level by default. The MODEM contact signal pins include: CTS pin, DSR pin, RI pin, DCD pin, DTR pin, RTS pin, all of which are at high level by default. All these MODEM communication signals can be used as general-purpose IO pins, controlled by MCU application program and their purposes can be defined.

CH438 has built-in independent transceiver buffer and FIFO, Support simplex, half-duplex or full duplex asynchronous serial communication. Serial data includes 1 low-level start bit, 8 data bits, 0 or 1 additional verification code or flag bit, 1 or 2 high-level stop bits, and supports odd/even/mark/blank checking. CH438 supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432m, 2.7648m, etc. The baud rate error of the serial port transmitting signal is less than 0.2%, and the allowable baud rate error of the serial receiving signal is not less than 2%.

CH438 can be used to extend additional high-speed RS232 for MCU/embedded system, high baud rate UARTs that support automatic hardware rate control, RS422 or RS485 communication interfaces, etc. through parallel ports. Existing serial port programs developed on the basis of industry standard 16C550 or 16C750 chip can be applied directly without any modification.

8. Parameters

8.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VCC=5V	-40	85	℃
		VCC=3.3V	-40	65	
TS	Ambient temperature during storage		-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)		-0.5	6.0	V
VIO	Voltage on the input or output pins		-0.5	VCC+0.5	V

8.2. Electrical Parameters

Test conditions: TA=25℃, VCC=5V

If the supply voltage is 3.3V, all current parameters in the table need to be multiplied by a factor of 40%.

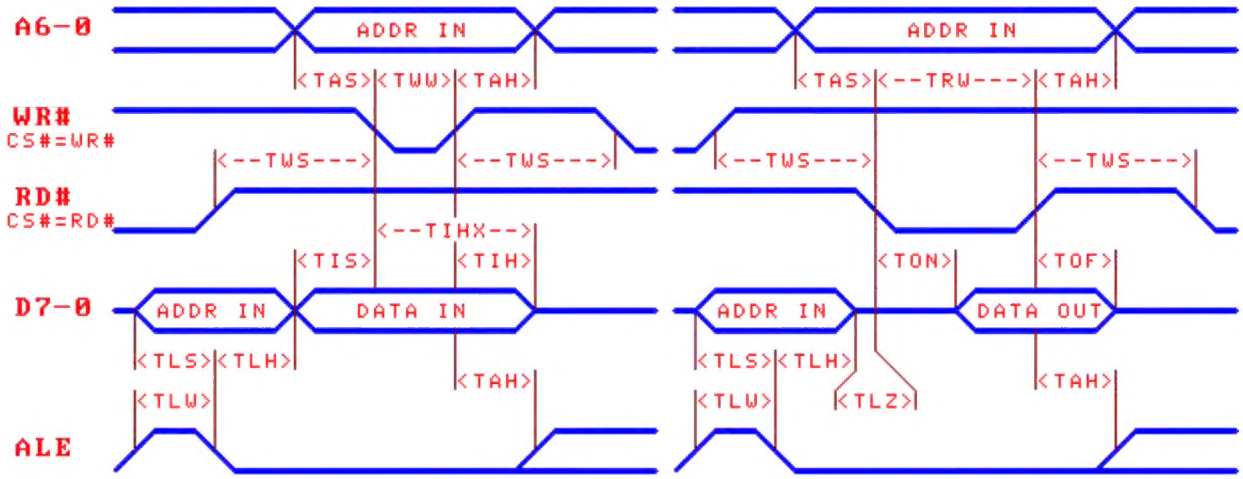
Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	3.3	5	5.3	V
ICC	Supply current during working at 5V	2	10	40	mA
ICC3	Supply current during working at 3.3V	0.5	5	20	mA
ISLP3	Supply current of 3.3V supply voltage during low-power sleep	5	50	500	uA
VIL	Low level input voltage	-0.5		0.8	V
VIH	High level input voltage	2.0		VCC+0.5	V
VOL	Low level output voltage (4mA draw current)			0.5	V
VOH	High level output voltage (2mA output current)	VCC-0.5			V
IIN	Input current of input terminal with built-in pull-down resistor			10	uA
IUP1	Input current at the input terminal with the weak pull-up resistor	2	5	170	uA
IDN1	Input current of input terminal with built-in weak pull-down resistor	-20	40	80	uA

8.3. Basic Timing Sequence

Test conditions: TA=25℃, VCC=5V; Parameter in Brackets VCC=3.3V, Refer to the Attached Drawing.

(RD means that the RD# signal is valid and the CS# signal is valid; WR#=1& RD#=CS#=0 performing a reading operation)

(WR means WR# signal is valid and CS# signal is valid, WR#=CS#=0 performing a writing operation)



Name	Parameter description	Min.	Typ.	Max.	Unit
FXI	XI input frequency, crystal frequency	0.9216	22.1184	32 (24)	MHz
TIC	Time from receiving clear interrupt operation to cancelling interrupt	2	20	100	nS
TWW	Width of effective strobe writing pulse WR	60 (120)			nS
TRW	Width of effective strobe reading pulse RD	50 (100)			nS
TWS	Interval width of strobe reading or strobe writing pulse	40 (80)			nS
TAS	Address input setup time before RD or WR	5 (8)			nS
TAH	Address input maintaining time after RD or WR	3			nS
TIS	Data input setup time before write strobe WR	0			nS
TIH	Data input maintaining time after strobe writing WR	10			nS
TIHX	Data input hold time on write strobe WR front edge	80	TWW + TIH		nS
TON	Effective strobe reading RD to effective data output		15 (25)	25 (40)	nS
TOF	Ineffective strobe reading RD to ineffective data output			20 (32)	nS
TLW	Width of effective address latch pulse ALE	6 (9)			nS
TLS	Address input setup time before address latch ALE	5 (8)			nS
TLH	Address input hold time after address latch ALE	3			nS
TLZ	Multiplexed address output is invalid until read strobe RD is valid	0			nS

9. Applications

9.1. Multiplexed Address Mode

AMOD pin of CH438 is at high level, using multiplexed address mode. ALE pin (pin A6) of CH438 is connected to ALE pin of MCU for inputting the latch enable signal of multiplexed address, and the pins A5-A0 can be suspended.

INT interrupt output pin of CH438 is an open-drain output pin, which shall be externally connected with a pull-up resistor (the recommended resistance is 2K-10K) before being provided to MCU.

RST# reset input pin of CH438 shall have active low power on reset signal and has a built-in weak pull-down resistor equivalent to 100KΩ. There are two signal sources available: one is that the RST# pin is connected with a 1KΩ-10KΩ resistor to the power supply and a 0.1uF-1uF capacitor to the ground to realize simple power on reset; the other is that MCU or other peripheral circuits provide power on reset or manual reset signal to RST# pin of CH438.

The clock frequency of XI pin of CH438 can be selected according to the maximum communication baud rate actually required. In order to reduce power consumption and electromagnetic radiation, it is recommended to select the lower frequency first, such as 7.3728MHz.

The serial port and MODEM signals of CH438 are at CMOS/TTL level, and eight RS232 can be realized by adding 75232/MAX213/ADM213/SP213/MAX3243 and other RS232 level converters.

CH438Q has no MODEM signal and can be used for a simplified three-line serial port.

9.2. Direct Address Mode

AMOD pin of CH438 is at low level, using direct address mode. The pins A6-A0 of CH438 are connected to the address bus of MCU for direct address input.